

Title: Mixed-Signal Circuit Design in Nanoscale CMOS

Speaker:

Dr. William Li
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Date: Friday, 10 September 2010

Time: 11:30 am – 12:30 pm

Venue: Room 603, Chow Yei Ching Building

Abstract:

CMOS scaling benefits digital circuits by providing faster logic switches with smaller area, but the improvements to analog/mixed-signal systems are less obvious; some even argue that CMOS scaling is hurting the performance. In this talk, we will look at scaling trends and the associated challenges to analog/mixed-signal circuit design as technology continues to scale. Illustrated with design cases, we show pathways to leverage scaling benefits to overcome the accompanied shortcomings. The required innovations combined with out-of-the-box thinking would make the design job all the more interesting.

Biography of the speaker:

William Li received a B.Eng in Computer Engineering from The University of Hong Kong, and M.S., M.Phil., and Ph.D. in Electrical Engineering from Columbia University. He was affiliated with IBM T. J. Watson Research Center, and now with Advanced Design, Intel Corp. He has been focusing on circuit design in leading-edge technologies including 65-, 45-, 32-, 22-nm and beyond. Having won twice in the IEEE ISLPED design contest, he is still interested in low-power design, particularly on PLL, ADC/DAC, and sensor interface.

Organizer: Prof. P.Y.S. Cheung