

Title: Graph-based Parallel and Statistical Analysis of Analog Circuits Based on GPU Platforms

Speaker:

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Abstract:

Modern computer architecture has shifted towards designs that employ multiple processor cores on a chip, so called multi-core processor or chip-multiprocessors (CMP). The graphic processing unit (GPU) is one of the most powerful many-core computing systems in mass-market use. In addition to the primary use of GPUs in accelerating graphics rendering operations, there has been considerable interest in exploiting GPUs for general-purpose computation (GPGPU). The introduction of new parallel programming interfaces for general purpose computations, such as Computer Unified Device Architecture (CUDA) has made GPUs powerful and attractive choice for developing high-performance numerical, scientific computation and solving practical engineering problems.

In this talk, I will present new parallel and statistical analog simulation techniques based on graph-based symbolic simulation techniques on GPU platforms. We show that determinant decision diagrams (DDD) based symbolic techniques are better suitable for GPU-based parallel computing than traditional numerical solutions such as LU decompositions. We propose data structures to present the DDD graphs in the GPUs for massively threaded parallel computing of the numerical values of DDD graphs. The new method explores data parallelism in the DDD numerical evaluation process where DDD graphs are traversed in depth-first fashion. We also extended our approach for Monte Carlo based statistical analysis based on newly organized data structure for fast memory access in GPU. Experimental results show that the new evaluation algorithm can achieve about one to two order of magnitudes

speedup over the serial CPU based evaluations of some analog circuits. The proposed statistical analysis method can outperform the numerical Monte Carlo simulation solutions using HSPICE. The proposed parallel techniques have potentials for the parallelization of many more decision diagrams based applications such as logic synthesis, optimization and formal verifications, which are based on binary decision diagrams (BDDs) and its variants.

Biography of the speaker:

Dr. Sheldon Tan received his B.S. and M.S. degrees in electrical engineering from Fudan University, Shanghai, China in 1992 and 1995, respectively and the Ph.D. degree in electrical and computer engineering from the University of Iowa, Iowa City, in 1999. He is a Professor in the Department of Electrical Engineering, University of California, Riverside, CA. He is the Associate Director of Compute Engineering Program (CEN) at Bourn College of Engineering at UC Riverside. He also is a cooperative faculty member in the Department of Computer Science and Engineering at UCR.

His research interests include statistical modeling, simulation and optimization of mixed-signal/RF/analog circuits, fast thermal analysis and modeling for microprocessors and platform systems, parallel circuit simulation techniques based on GPU and multicore systems, and embedded system designs based on FPGA platforms. He also co-authored book "Symbolic Analysis and Reduction of VLSI Circuits" by Springer/Kluwer 2005 and "Advanced Model Order Reduction Techniques for VLSI Designs" by Cambridge University Press 2007. Dr. Tan now is serving as an Associate Editor for three journals: ACM Transaction on Design Automation of Electronic Systems (TODAE), Integration, The VLSI Journal, and Journal of VLSI Design.

Dr. Tan received Outstanding Oversea Investigator Award from the National Natural Science Foundation of China (NSFC) in 2008. He received NSF CAREER Award in 2004. Dr. Tan received the Best Paper Award from 2007 IEEE International Conference on Computer Design (ICCD'07), two Best Paper Award Nomination from 2005 and 2009 IEEE/ACM Design Automation Conferences, the Best Paper Award from 1999 IEEE/ACM Design Automation Conference. He served as a technical program committee member for DAC, ICCAD, ASPDAC, ICCD, ISQED, BMAS, ASICON.

Organizer: Dr. N. Wong