Computational Scaling Technology (CST) and Design-Technology Co-optimization (DTCO) – The advancement for the scaling of semiconductor design

Details

Speaker:
Dr. Kafai Lai Semiconductor Research & Development Center IBM

Date:
Wednesday, 24 March 2010

Time:
10:30am - 11:30am

Venue:
Room 603, Chow Yei Ching Building

Abstract:

For decades lithography has been a key driver enabling the continued scaling of semiconductor technology. The ability to print smaller features generation after generation has been achieved by means of better lithography tools with improved numerical aperture (NA) and/or shorter wavelength, advanced resolution enhancement techniques and better mask and process technology. As we look into the 22nm node and beyond, the industry faces a lithography tooling discontinuity. Having reached the NA limits of water-based 193nm optical lithography, and with EUV still faces some technical and timing challenges, the industry is faced with the daunting challenge of providing a 70% node-to-node linear shrink (while still meeting a two-year cycle) in the absence of any new tool offering either an increase in numerical aperture or a wavelength decrease. Computational Scaling Technology is a comprehensive strategy to enable the continued functional scaling of semiconductors in the presence of such a discontinuity. The strategy revolves around the co-optimization of design and process technology to enable an optimum trade-off between manufacturability and design capabilities, with mathematical optimization, automation and high-performance computing as key enablers.

Biography of the speaker:

Dr. Kafai Lai, obtained his BSc. (hon) from the University of Hong Kong in 1988 and his MS and PhD degrees from the University of Texas at Austin in 1992 and 1995 respectively, all in electrical engineering. Dr. Lai has been working in the field of Photolithography and Design technology Co-optimization R&D since graduation for 15 years after graduation. He worked in Rockwell Semiconductor and Texas instruments as a member of technical staff. Since 1999 he has been working in the Semiconductor

Research and Development Center at IBM. His research focus was in optical imaging modeling, lens characterization, exposure tooling analysis, OPC model improvement and lithography/RET development. Currently he is developing software and hardware solution to enable design scaling using Source Mask optimization (SMO) as well as Design Technology Co-optimization (DCTO). He has successfully led several multi-company Joint R&D programs with vendors and academia and has involved in writing proposals for external research grant (such as DARPA) as well. Dr. Lai has been recognized as a world class technical leader in the field has been serving in the technical program committee of the top Lithography conference worldwide (SPIE Advanced Optical Lithography Conference) since 2005 as well as the lithography Symposium Chair for the CSTIC conference in Shanghai since 2009. He has given several invited papers in major conferences worldwide on topics like, and offered short courses in optical lithography modeling in many advanced lithography conferences. Dr. Lai has authored and co-authored >50 technical papers and have >36 patents granted worldwide.

Enquiries: kitty@eee.hku.hk