Standard cell design with regularly-placed contacts and gates

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ABSTRACT

The layout strategies of standard cells with regularly-placed contacts and gates are studied. The regular placement enables more effective use of resolution enhancement technologies, which in turn allows a reduction of critical dimensions. Although regular placement of contacts and gates adds restrictions during cell layout, the overall circuit area can be made smaller and the number of extra masks and exposures can be kept to the lowest by careful selection of the grid pitch, using template-trim lithography method, allowing random contact placement in the vertical direction, and using rectangular rather than square contacts. Three different fabrication-friendly layouts are compared in this study. The average area change of 64 standard cells in a 130 *nm* library range from −4.2% to −1.2% with the 3 fabrication-friendly layout approaches. The area change of 5 test circuits using the 3 approaches range from −5.4% to +2.6%. Power consumption and intrinsic delay also improve with the decrease in circuits area, which is verified with the examination results.

Keywords: Low-k_1 lithography, Resolution Enhancement Technologies, Fabrication-friendly layout, Multiple exposures, Template lithography, Standard cells, Power consumption, Circuit delay

1. INTRODUCTION

The continuous demand for high speed integrated circuits (ICs) results in the continuous increase of transistor density and decrease of the feature size in the past two decades. The critical dimension (CD)—the minimum feature size that can be defined by optical lithography—has been reduced to 130 nm at the end of the last century and is projected to reach the 65 nm node in 2007.[1] As a function of three parameters, the CD ($= k_1 \frac{\lambda}{\mathrm{NA}}$) is proportional to the wavelength of the exposure light λ and the process-related factor k_1, and decreases with increasing numerical aperture (NA) of the projection system. Over the past two decades, the development of optical lithography has been successful in reducing the λ from 436 nm in the 1970s to 157 nm in 2004 and increasing the NA to above 0.85.[2] However, these improvements alone are insufficient to reduce the feature size exponentially as projected by Moore's law.[3]

As the third parameter and the best measure of lithography aggressiveness, the k_1 factor is the only parameter that can be controlled by lithographers for a given exposure system. The theoretical lower limit of the k_1 factor is 0.25.[2] Over the past two decades, the k_1 factor has been reduced by over 0.1 every 5 years.[4] Because image quality degrades noticeably when k_1 falls below 0.75, resolution enhancement techniques (RETs) such as modified illumination,[5] optical proximity correction (OPC),[6] and phase-shifting masks (PSMs)[7] have been used to improve image quality for low-k_1 lithography. These RETs have been successful in reducing the k_1 factor to about 0.5.[8] However, with k_1 approaching its limit, the additional improvement requires communications between the technology and the design communities. By considering circuit manufacturability in the layout design, it is expected that the k_1 factor can be further reduced by fabrication-friendly layout in which the circuit pattern configurations are limited to facilitate lithography optimization.

For example, gate and contact level are the most difficult part of a lithography process and have the biggest cost weighting. Many advanced lithography approaches have been proposed in the last few years for the contact

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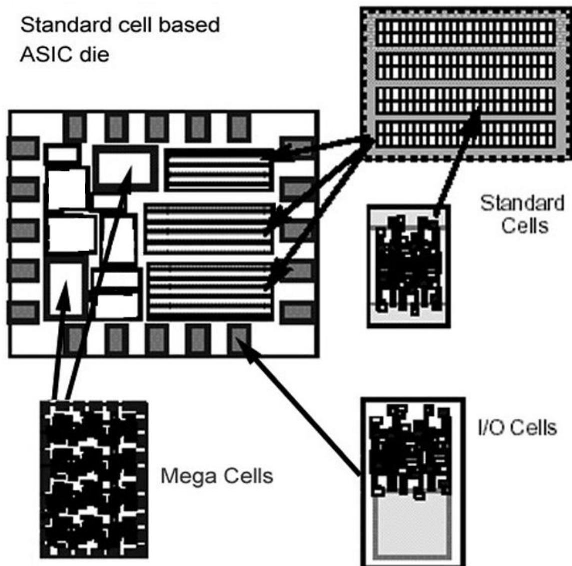

Figure 1. A cell-based ASIC die typically consists of three types of cells: I/O cells, mega cells (memory or micro-controllers, etc.), and standard cells (AND gates, OR gates, and flip-flops, etc.).[9]

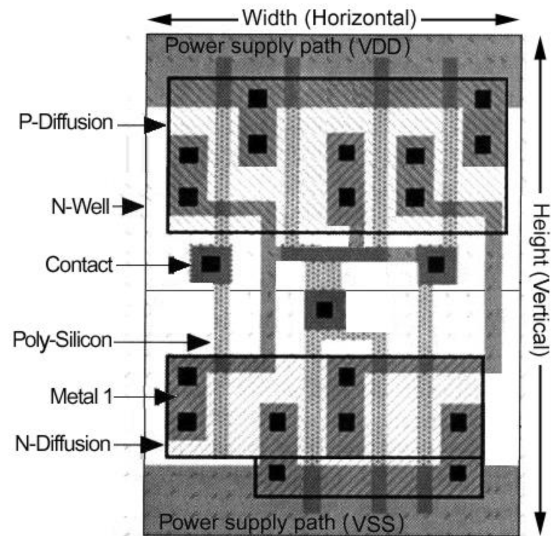

Figure 2. Structure of a typical standard cell composed of 6 layers: N-well, N-diffusion, P-diffusion, poly-silicon, contact and metal-1. The first 4 layers are primarily used to construct the MOSFETs while the latter 3 layers are used for intra-cell connections.

and the gate level,[10–16] pushing the k_1 to about its minimum value.[11] All of these approaches require a regularly placed contacts or gates.

There is a trade-off between randomly-placed (traditional) and regularly-placed (fabrication-friendly) layout. Excessive lithography friendliness may be so restrictive on layout compaction that circuit area increases unacceptably. Although the features can be designed smaller and packed closer in regularly-placed layout, the initial area increase should be small enough such that it can be offset by shrinkage of the feature size.

It is reasonable to expect that whether a circuit area will be smaller or not after using a fabrication-friendly layout depends on the applications. In this study, we examine the application of regularly-placed contacts and gates on standard cells in application-specific integrated circuit (ASIC) design.

2. LAYOUT DESIGN

A cell-based structure is an important structure for ASIC design. A cell based ASIC die typically consists of three types of cells: I/O cells, mega cells, and standard cells, as shown in Fig. 1. As one of the core blocks of a cell-based ASIC, standard cells are used here to demonstrate the application of regularly-placed contacts and gates on ASIC design. A 130 nm standard cell library is used in this study to demonstrate the effects.

Fig. 2 shows the structure of a typical standard cell. Each standard cell in a library is rectangular with a fixed height but variable width. MOSFETs are placed one by one in the horizontal direction with vertical-oriented gates.

We have previously reported our efforts to place contacts regularly in a standard cell layout.[17] The grid pitches should be selected carefully to keep the final circuit area smaller. All contacts were placed on a grid with the $\frac{1}{2}$ transistor pitch* as the horizontal grid pitch and the $\frac{1}{2}$ metal-1 pitch as the vertical grid pitch in that study. The gates of MOSFETs were placed randomly.

*A transistor pitch, also called a "contacted pitch", is the minimum pitch between two gates with a contact between them.

2.1. Horizontal grid pitch

In reality, the placement of contacts and gates in the horizontal direction are correlated in a standard cell layout and should be considered simultaneously. As shown in Fig. 3, which is a typical layout block in a standard cell, the contacts $C1 - C4$, and gates $G1 - G3$ are interlaced. Gates are just placed in the middle of contacts. All these contacts and gates are on grid already if a $\frac{1}{2}$ transistor pitch is used as the horizontal grid pitch. No area increase is needed to put these contacts and gates on grid horizontally. This can also be explained using the average[†] pitch distributions of gates and contacts, as shown in Fig. 4 and Fig. 5 respectively. The highest peaks of the both distributions (p_1 in Fig. 4 and p_4 in Fig. 5) are in the same position and equal to one transistor pitch.

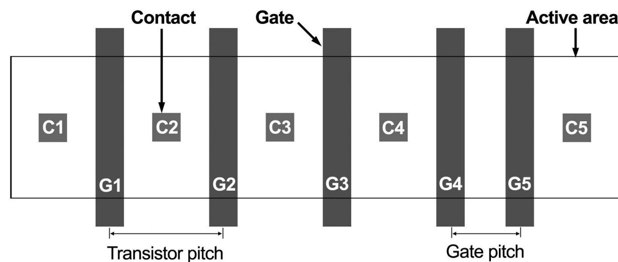

Figure 3. A typical layout block of neighboring MOSFETs in a standard cell.

However, it would be different if there are more than one gate in the middle of two contacts, such as the gates $G4$ and $G5$ in Fig. 3. The two-gate scenario is common in both sequential and combinational cells, represented as the peak p_2 in Fig. 4 and p_3 in Fig. 5 respectively. The three- and four-gate scenario are often found in multiple-input combinational cells, such as 3- and 4-input NAND gates or NOR gates. Typically the gate pitch[‡] is mismatched with the transistor pitch (ranges from $\frac{1}{2}$ to 1 transistor pitch). The gate pitch must be enlarged to one transistor pitch when placing the neighboring gates on the grid. That leads to an area increase. Although the CD reduction results from the regular feature placement might offset the initial area increase and end up with a smaller final cell area, a smaller initial area increase is still needed.

Even so, the transistor pitch must still be used as the horizontal grid pitch (or multiple of the horizontal grid pitch) because it represents the highest peak in both the gate and the contact pitch distributions (Fig. 4 and Fig. 5). By adding the placement of gate contacts into the consideration,[17] a $\frac{1}{2}$ transistor pitch is used as the horizontal grid pitch for both contacts and gates when placing them regularly in the horizontal direction. The grids of contacts and gates are uniform.

2.2. Vertical placement

Placing features regularly in a direction facilitates the optimization of a lithography process in that direction and leads to a reduced feature size. On the other hand, the extra restrictions in layout increase the complexity of a design and might offset the benefits from the reduced CD. That means whether to apply the regular layout placement on one kind of features in a direction depends on how the CD of these features affects the cell area in that direction. Because MOSFETs are placed one by one horizontally in a standard cell, such as those shown in Fig. 3, the width of a cell is roughly determined by the product of the transistor pitch and the number of the transistors. The reduction of the minimum contact and gate size gets a reduced transistor pitch and leads to a decrease in the cell width. On the other hand, it is the metal-1 pitch instead of the contact pitch that determines the height of a standard cell[§]. Applying a fabrication-friendly design on the contact layer in the vertical direction cannot help to decrease the height of a standard cell. Fabrication-friendly layout must be applied on metal-1 layer to decrease the height. However, multiple exposures are needed to fabricate the regularly-placed layout.[17]

[†]We have an average distribution of 30 standard cells in this study.

[‡]A gate pitch, also called a "non-contacted pitch", is the minimum pitch between two gates without contacts between them.

[§]The typically height of a standard cell is 10 metal-1 pitches: 3 pitches for power supply paths and 7 pitches for intra-cell routing.[17]

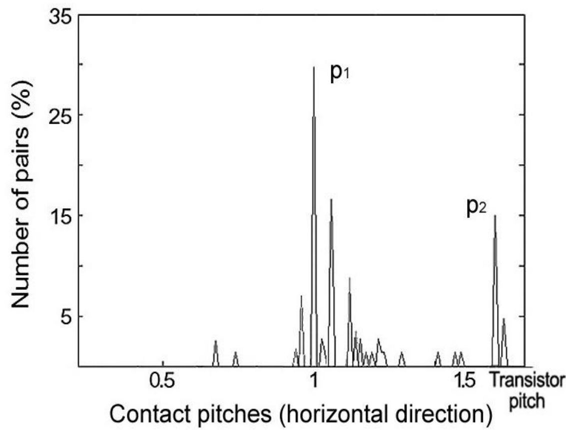

Figure 4. Average horizontal contact pitch distribution of standard cells.

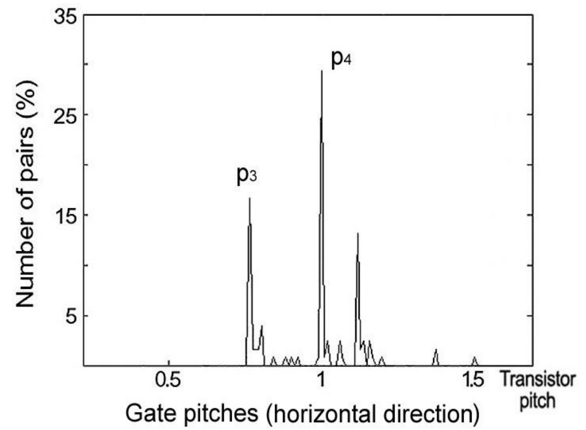

Figure 5. Average horizontal gate pitch distribution of standard cells.

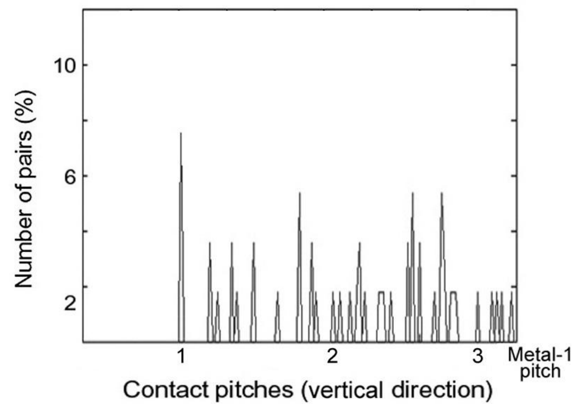

Figure 6. Average vertical contact pitch distribution of standard cells.

The more layers on which regular placed layout is applied, the more extra masks and exposures are need. As will be described in Sec. 3, about five exposures are needed altogether for the lithography of the regularly-placed contacts and gates. More exposures may not be practical from an economics point of view.[18]

As shown by the average vertical pitch distributions of contacts(Fig. 6), there is no a dominant peak in the pitch distribution. That means the original placement of contacts are quite random in the vertical direction. Placing them regularly in the vertical direction increases the restriction during layout design and offsets some length decrease resulted from the regular placement in the horizontal direction. Therefore, it would better to keep the vertical placement of contacts randomly.

The case of gates is more complicated than that of contacts. Besides gates, there are still connection paths and contact-landing pads in a poly-silicon layer. Mostly, MOSFETs are designed one by one horizontally in a standard cells with vertical-oriented gates, such as the gates in Fig. 3. The vertical dimension of a gate (width) is not as critical as the horizontal dimension (length). It is no necessary to apply the fabrication-friendly layout on gates in the vertical direction. At the same time, although the vertical dimension (width) of horizontal-oriented poly-silicon connection paths can be reduced by a regular placement of them in the vertical direction, it is not helpful to reduce the height of a standard cell except for an increased difficulty in the layout compaction. A random placement is better for horizontal-oriented poly-silicon connection paths, like the case of contacts.

3. LITHOGRAPHIC APPROACHES

From the discussion above, it can be concluded that the placement of contacts and gates should be kept random in the vertical direction while regular in the horizontal direction with $\frac{1}{2}$ transistor pitch as the grid pitch. However, there are several difficulties to apply such a fabrication-friendly layout on a standard cell. Firstly, it is difficult to keep contacts randomly in the vertical direction while placing them regularly in the horizontal direction. All of the approaches in the literature placed contacts regularly in both directions at the same time.[13,14,17] Secondly, although the horizontal resolution (single-exposure) can be improved by a fabrication-friendly layout, the desired horizontal grid pitch ($\frac{1}{2}$ transistor pitch) is still smaller than the improved resolutions of both contact and gate layers. Multiple exposures must be introduced to fabricate the new layout.[17] This increases the cost and decreases the throughput. The lithographic approach should be selected carefully to decrease the number of extra masks and exposures.

Many lithographic approaches have been proposed for the regularly-placed layout.[12–14,16–18] There are mainly two kinds: assist feature approaches[14,17] and template-trim mask approaches.[12,13,16,18] Assist features are added around isolated features in assist feature approaches to improve the process latitude. Regularly-placed layout facilitates the optimization of assist feature approaches,[10] which is one of the initial motivations to place features regularly. The advantage of assist feature approaches is they can be implemented by one exposure while multiple exposures must be used for template-trim mask approaches. However, as described above, a sub-resolution pitch must be used to prevent the increase of cell area. Multiple exposures is unavoidable, even for assist feature approachs. Considered that the contacts and gates use the same horizontal pitch, template-trim approaches is a good choice to decrease the number and cost of masks.[18] A reusable template mask can be applied for both contact and gate layers to form an array of fine patterns, and two trim masks are used for the two layers to remove the unwanted parts. Although the number of exposures may not be fewer than that of assist feature approaches, the number and cost of masks are decreased. Furthermore, by using a chromeless alternate phase-shifting template mask, the minimum feature size and pitch can be decreased to much smaller than those of assist feature approaches.[11] At the same time, by using the same template mask for contacts and gates, the match between the transistor pitch and gate pitch eliminates the extra area increase during a redesign of standard cells with neighboring gates. This extra area increase is caused originally by the mismatch of the two pitches (Sec. 2.1).

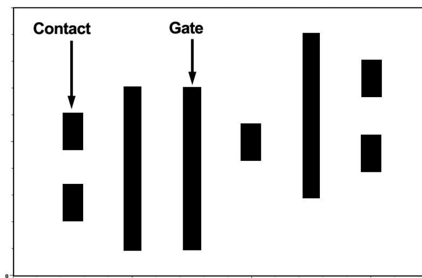

Figure 7. A test layout block.

Several template-trim lithographic approaches, such as MIT Lincoln Laboratory GRATEFUL method[18] and Canon IDEAL method,[12] can be used to fabricate the poly-silicon layer of a fabrication-friendly standard cell. However, the current template-trim approaches[11,13,16] for contacts should be modified when applied to the contact layer of a fabrication-friendly standard cell. These methods use a triple-exposure approach. Two exposures of template mask form a matrix of small contact holes and a third exposure of a trim mask removes the unwanted contact holes from the matrix. The contact size reaches the minimum in both the horizontal and the vertical directions. However, as described in Sec. 2.2, random placement of contacts in the vertical direction is preferred for a standard cell and the vertical contact size is not critical for the area of a standard cell. A novel lithographic approach is proposed in this study[19] for the contact layer of a fabrication-friendly standard cell. Rectangular-size contacts, with the minimum size in the horizontal direction, are placed randomly in the vertical direction and regularly in the horizontal direction. Two masks (a template mask and a trim mask) and

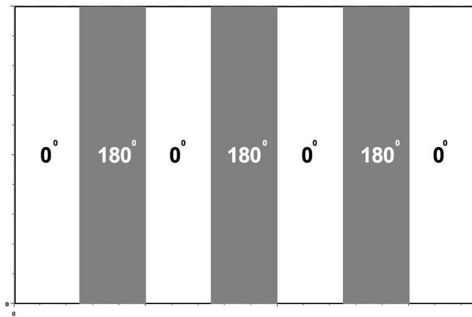

Figure 8. The chromeless alternating phase-shifting template mask.

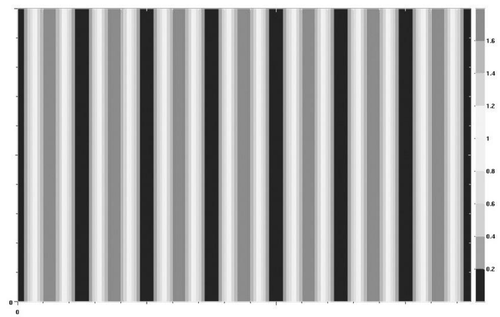

Figure 9. The lithographic image of the chromeless alternating phase-shifting template mask.

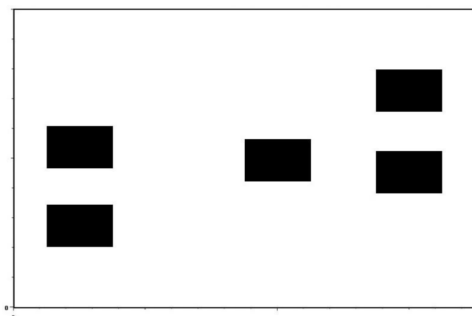

Figure 10. The trim mask for contacts.

Figure 11. The binary trim mask for gates.

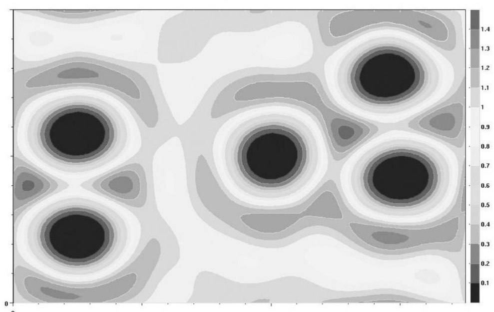

Figure 12. The lithographic image of the trim mask for contacts.

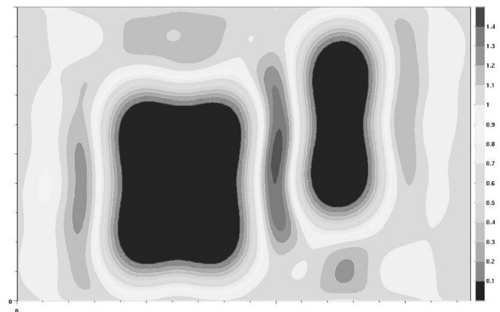

Figure 13. The lithographic image of the binary trim mask for gates.

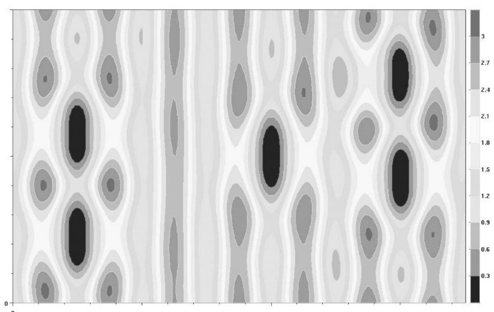

Figure 14. The final image of the contacts.

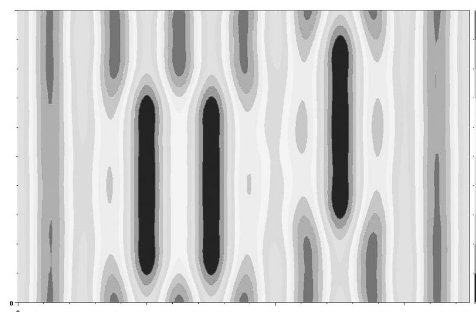

Figure 15. The final image of the gates.

two exposures are needed for the new lithographic approach. Note that there are three masks (two template masks¶ and a trim mask) and three exposures are needed for the original template-trim approach. The new approach decreases the fabrication cost and the layout restrictions at the same time.

To fabricate the layout of contacts and gates as shown in Fig. 7 for example, we need one reusable chromeless alternating phase-shifting template mask (Fig. 8) and two trim masks for contacts (Fig. 10) and gates (Fig. 11) separately. All contacts and gates are placed randomly in the vertical direction while regularly in the horizontal direction with $\frac{1}{2}$ transistor pitch as the grid pitch. A $\lambda = 193\,\text{nm}$, NA=0.75 lithography system and a 245 nm horizontal pitch ($\frac{1}{2}$ transistor pitch) are used in this investigation. After an exposure, the opposite phase shift of patterns on the chromeless template mask creates periodic unexposed dark lines at the boundary of 0° and 180° regions, as shown in Fig. 9. The period of the 0° and 180° regions on the chromeless phase-shifting template mask is design to be one transistor pitch so that the period of the dark lines is half of that. Exposures of the contact and gate trim mask (Fig. 12 and Fig. 13) on these period dark lines remove the unwanted parts of the dark lines and the cuts of the dark lines left form the final images of regularly-placed contacts (Fig. 14) and gates (Fig. 15).

The horizontal dimension and position of contacts and gates are determined by the exposure of the template mask, while the vertical dimension and position are determined by the trim mask. Because the features in the trim mask are placed randomly, the positions of contacts and gates are randomly in the height direction. Determined by the exposures of the different masks, contacts have different size in different directions. By using the regular placement and the chromeless phase-shifting mask in the horizontal direction, the horizontal contact size is smaller than the vertical contact size which is determined by the resolution of the contact trim mask. The horizontal size of a contact can be as small as that of a gate. For example, a 70 nm $\sim$ 80 nm horizontal contact size can be reached using a 193 nm lithography.[11] Although a binary trim mask can be used for gates because of their relatively larger dimension in the vertical direction, an advanced trim mask should be used to get a vertical contact size the same as the minimum contact size of tradition one-exposure approaches, which is 160 nm in a 193 nm lithography. The original transistor pitch of a 193 nm lithography is about 510 nm. Using an optimized assist feature approach, it can be decreased to about 490 nm. Although the transistor pitch can be reduced to much smaller than 490 nm by using template-trim approaches, further study is still needed to determine the minimum transistor pitch for standard cells enabled by template-trim approaches.

The double-exposure template-trim approach proposed can only form gate features. Another layer of resist and exposure is still needed to form other features in a poly-silicon layer, such as the horizontal-oriented poly-silicon connection paths and contact landing pads whose dimension is not critical and can be printed large than that of gates. Many other template-trim approaches can also be used to fabricate a poly-silicon layer.[11, 12, 15, 18]

There are altogether 4 masks (1 reusable template mask, 1 trim mask for contacts, 1 trim mask for gates, and 1 mask for other features on a poly-silicon layer) and 5 exposures (2 for a contact layer and 3 for a poly-silicon layer) are needed to fabricate the contact and poly-silicon layer of the new standard cell in this study. The extra cost is kept to the lowest because only one extra non-reusable mask is needed and no non-reusable mask needs advantage fabrication technology.

4. EXPERIMENTAL RESULTS

Sixty-four standard cells in a 130 nm technology library are redesigned using the fabrication-friendly layout. To compare the effects of different approaches on cell area, the cells are redesigned using 3 different approaches: 1. Contacts and gates are placed regularly only in the horizontal direction. Use the template-trim approach, with $P_x = 245\,\text{nm}$ ($\frac{1}{2}$ transistor pitch). 2. Same as the approach 1 except that contacts are placed regularly in the both directions. Use $\frac{1}{2}$ metal-1 pitch as the vertical grid pitch. 3. Same as the approach 2 except for using assist feature approaches. The gate pitch is equal to the grid pitch in approach 1 and 2 while larger than the grid pitch in approach 3. The height of the cells are kept unchanged. Adjustments in cell area are represented by the change of cell widths. Cell area changes are plotted in Fig. 16 – Fig. 18, which show the histogram of percentage of relative area change for the 64 cells.

¶Since the preferred grid pitches of contact layer in the two directions are different when contacts are placed regularly

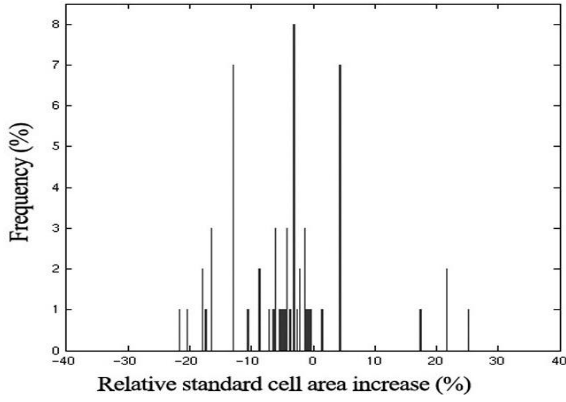

Figure 16. Histogram of percentage area change of the 64 standard cells in approach 1. The average cell area change is −4.2%.

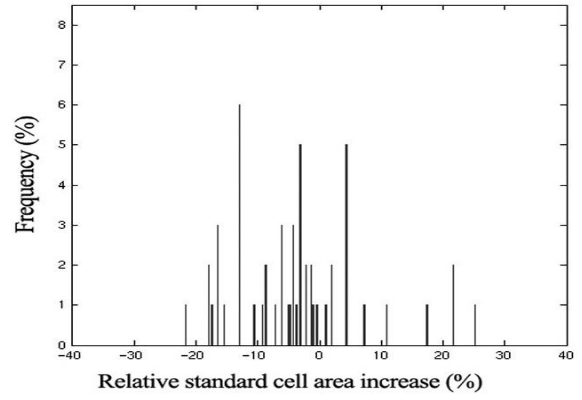

Figure 17. Histogram of percentage area change of the 64 standard cells in approach 2. The average cell area change is −3.0%.

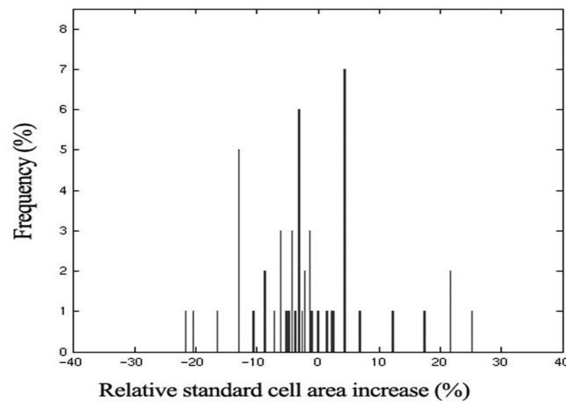

Figure 18. Histogram of percentage area change of the 64 standard cells in approach 3. The average cell area change is −1.2%.

Table 1. Relative area change ($\frac{Area_{new} - Area_{old}}{Area_{old}} \times 100\%$) of 5 circuit blocks designed using the fabrication-friendly standard cells of the 3 different approaches described in Sec. 4. The height of cells are kept unchanged. A 130 nm technology is used for this examination.

Circuit blocks	Area change (Approach 1)	Area change (Approach 2)	Area change (Approach 3)
Finite impulse response (FIR) filter	−5.1%	−3.5%	−2.2%
Trace-back unit (TBU) in Viterbi decoder	−5.4%	−4.1%	−1.8%
Add-compare-select (ACS) unit in Viterbi decoder	−4.4%	−2.6%	+1.2%
Adder register block	−2.1%	+0.9%	+2.0%
Signal-to-noise ratio (SNR) detector in CDMA decoder	+0.4%	+1.9%	+2.6%

The average area change of the 3 approaches are −4.2%, −3.0%, and −1.2% respectively. The cell area change ranges roughly from −25% to +25% in these approaches. With the same horizontal grid pitch, placing contacts randomly in the vertical direction (approach 1) get an average cell area about 1.2% smaller than that with contacts placed regularly in the vertical direction (approach 2). With the same horizontal and vertical grid pitch, the mismatch between the gate pitch and the transistor pitch when use assist feature approaches (approach 3) leads to an extra 1.8% area increase comparing with that of the cells with two pitches matched when use template-trim approaches (approach 2).

Since different circuits use different combination of standard cells, changes in circuits area vary from circuit to circuit. Five circuits are designed using the fabrication-friendly standard cells to study the effects on circuit area. Circuits are also designed using the 3 different approaches of the fabrication-friendly layout for a comparison, as shown in Table. 1. It is found that the final area of a circuit strongly depends on the standard cells it has and can differ a lot. The area of some test circuit increases after using the new layout style. Except for approach 3, the other two approaches lead to a smaller average circuit area. Roughly, the average cell area increase can be used as an index for average circuit area increase. Template-trim approaches are preferred to assist feature approaches for standard cells.

5. CIRCUIT PERFORMANCES

Power consumption and intrinsic delay of a standard cell, which are determined by the layout, also change with the application of a fabrication-friendly layout. Since the new standard cells are modified on the base of the original cells, the power consumption and intrinsic delay of a new cell can be estimated according to the change of the cell layout.

5.1. Theoretical estimation

Circuit power consumption and intrinsic delay depend on parasitic capacitance and transistor gain factor. Roughly, their relations can be represented as below[20]:

$$P \propto C_L, \tag{1}$$

$$D \propto \frac{C_L}{k}, \tag{2}$$

where P and D are the power consumption and the intrinsic delay of a standard cell respectively. C_L and k are the total parasitic capacitance and average transistor gain factor of a cell. The C_L and k can be estimated using the equations below:

$$C_L = C_g + C_o, \tag{3}$$

$$k \propto \frac{W}{L}, \tag{4}$$

where C_g is the parasitic capacitance of gates, and C_o is the parasitic capacitance of all other sources. As the two parts of parasitic capacitance, C_g and C_o contribute approximately equally to the total parasitic capacitance. W and L are the width and the length of a gate.

To keep the analysis simple, widths of gates and the height of cells are kept unchanged when redesign standard cells. Set $\Delta = \frac{Area_{new}}{Area_{old}}$ as the relative area of a new cell and $\gamma = \frac{L_{new}}{L_{old}}$ as the gate length reduction ratio. Using the derivation in Appendix A, the relative power consumption and intrinsic delay of a new cell can be represented as the equations below:

$$\frac{P'}{P} \approx \frac{\alpha+1}{2} + \frac{\beta}{2} \cdot (\Delta - 1), \tag{5}$$

$$\frac{D'}{D} \approx \gamma \cdot \left[\frac{\alpha+1}{2} + \frac{\beta}{2} \cdot (\Delta - 1)\right], \tag{6}$$

in the two directions,[17] two different template masks are needed for the original template-trim approaches.[11,13,16]

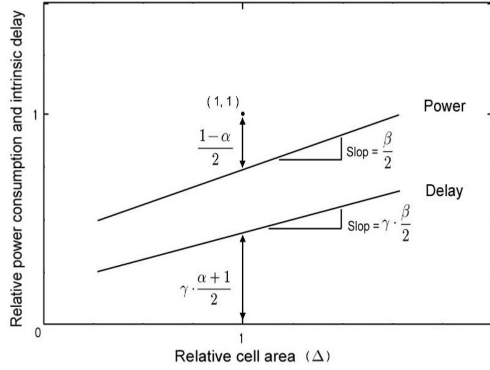

Figure 19. The relative power consumption and intrinsic delay can be treated as first-order functions of the relative cell area Δ.

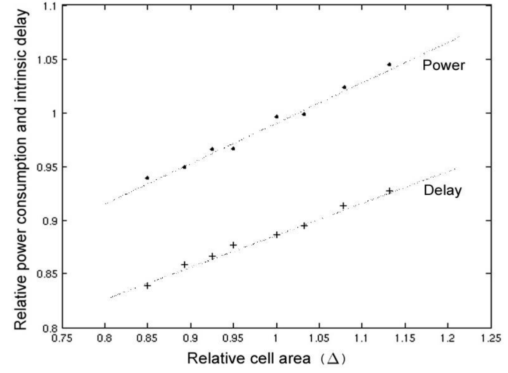

Figure 20. Examination results of 8 standard cells. The relative power consumption and intrinsic delay are roughly first-order functions of the relative cell area Δ.

where P' and D' are the power consumption and intrinsic delay of a new cell. α ($\alpha > 0$) is a function of γ and can be treated as a constant when the gate length reduction ratio is fixed. β ($0 < \beta < 1$) represents how much of C_o is proportional with the cell length and can also be treated as a constant.

From Equ. 5 and Equ. 6, it can be concluded that the relative power consumption and intrinsic delay are first-order functions of the relative cell area when the gate length reduction ratio is fixed, as plotted in Fig. 19. The slops are $\frac{\beta}{2}$ and $\gamma \cdot \frac{\beta}{2}$ respectively. Both of them are smaller than $\frac{1}{2}$. The relative power consumption and intrinsic delay decrease with the decrease of cell area. The same conclusion can be gotten for other cases using similar derivations which will not be described in this paper.

5.2. Examination results

The relative power consumption and intrinsic delay of 8 fabrication-friendly standard cells in a 130 nm library are examined. The gate length reduction ratio is 0.9. The height of cells is fixed and the width of all gates are kept unchanged. The result, as plotted in Fig. 20, fits the estimation in Sec. 5.1 very well. The points of the relative power consumption and intrinsic delay form roughly two lines in Fig. 20. $\alpha \approx 0.97$ and $\beta \approx \frac{2}{3}$. The slops are $\frac{1}{3}$ and $\frac{0.9}{3}$ respectively.

6. CONCLUSIONS

Fabrication-friendly layout does not necessarily mean an increase of circuit area and fabrication cost. With the carefully selected grid pitch and lithographic approach, the circuit area can be made smaller and the number of extra masks and exposures can be kept to the lowest. The using of template-trim lithographic method and the introducing of rectangular rather than square contacts make it possible to get a decreased circuit area when apply the regularly-placed contacts and gates in the standard cell layout. Circuit performance improves with the decrease of the circuits area.

APPENDIX A. DERIVATION OF ESTIMATION EQUATIONS FOR RELATIVE POWER CONSUMPTION AND INTRINSIC DELAY OF FABRICATION-FRIENDLY STANDARD CELLS

According to Equ. 1 and Equ. 2, the relative power consumption and intrinsic delay of a standard cell can be represented as

$$\frac{P'}{P} = \frac{C'_L}{C_L}, \tag{7}$$

$$\frac{D'}{D} = \frac{C'_L}{C_L} \cdot \frac{k}{k'}, \tag{8}$$

where C'_L and k' are the total parasitic capacitance and the average transistor gain factor of a new cell. $\gamma = \frac{k}{k'}$ is typically fixed during the redesign of the cells. For example, when widths of gates are kept unchanged, γ can be represented as: $\gamma = \frac{L_{new}}{L_{old}}$ and be a constant. Therefore, the estimations of $\frac{P'}{P}$ and $\frac{D'}{D}$ are simplified as the estimation of $\frac{C'_L}{C_L}$.

As represented in Equ. 3, the C_L consists of C_g and C_o. Both of them are roughly half of C_L. To estimate the change of C_L after the redesign, we make two assumptions:

1. C_g is only determined by the size of gates. Since the size of gates is fixed no matter how the cell area increase, the $\frac{C'_g}{C_g}$ is only a function of γ and can be treated as a constant during a redesign, where C'_g is the average transistor gain factor of a new cell. We set

$$\alpha = \frac{C'_g}{C_g}. \tag{9}$$

2. When the height of cells is fixed during a redesign, cells only stretch in the horizontal direction. The C_o, which is determined by the area of cells, can be treated as a first-order function of relative area $\Delta = \frac{Area_{new}}{Area_{old}}$ and be represented as:

$$C_o = C_{o1} + C_{o2}, \tag{10}$$

where C_{o1} is the part of C_o that is not changed with the stretch of standard cells in the horizontal direction and C_{o2} is the other part of C_o that is proportional to the width of a cell. Set

$$C_{o2} = \beta C_o, \ (0 < \beta < 1). \tag{11}$$

Therefore,

$$C'_o = C'_{o1} + C'_{o2} = C_{o1} + \Delta \cdot C_{o2} = C_{o1} + \beta \cdot \Delta \cdot C_o, \tag{12}$$

where C'_o, C'_{o1} and C'_{o2} are C_o, C_{o1} and C_{o2} of a new cell.

Substitute the Equ. 3 and Equ. 9–12 into Equ. 7 and Equ. 8, we get:

$$\begin{aligned}
\frac{P'}{P} &= \frac{C'_L}{C_L} \\
&= \frac{C'_g + C'_{o1} + C'_{o2}}{C_L} \\
&= \frac{C'_g + C_{o1} + \Delta C_{o2}}{C_L} \\
&= \frac{C'_g + C_{o1} + C_{o2} + (\Delta - 1)C_{o2}}{C_L} \\
&= \frac{\alpha C_g + C_o + (\Delta - 1)\beta C_o}{C_L} \\
&= \alpha \frac{C_g}{C_L} + \frac{C_o}{C_L} + (\Delta - 1)\beta \frac{C_o}{C_L} \\
&\approx \frac{\alpha + 1}{2} + \frac{\beta}{2}(\Delta - 1). \qquad (13) \\
\frac{D'}{D} &= \gamma \frac{C'_L}{C_L} \\
&\approx \gamma \left[\frac{\alpha + 1}{2} + \frac{\beta}{2}(\Delta - 1) \right]. \qquad (14)
\end{aligned}$$

Because α, β, and γ are roughly constants during a redesign, the relative power consumption and intrinsic delay can be treated as first-order functions of the relative cell area Δ.

In some redesigns, the height of cells and the gate widths W are changed. Because the new height is fixed for all cells and if $\frac{W_{new}}{W_{old}}$ is fixed for all gates, the relative power consumption and intrinsic delay will also be first-order functions of the relative cell area Δ.

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