Curriculum Vitae

Hayden Kwok Hay So

8E Hillwood Court, 22-28 Hillwood Road, TsimShaTsui, Kowloon

hso@eee.hku.hk

Research Interests

- Operating system design for reconfigurable computing platforms.
- Reconfigurable computer architectures, models and HW/SW codesign methodologies.
- Application of reconfigurable computing to biomedical engineering, embedded system and network security.

Education

University of California, Berkeley Aug 2002 – Dec, 2007
Ph.D in Electrical Engineering and Computer Sciences
Thesis title: "BORPH: an operating system for FPGA-based reconfigurable computers."

University of California, Berkeley Aug, 1998 – Dec, 2000
M.S. in Electrical Engineering and Computer Sciences
Thesis title: "BEE: A reconfigurable emulation engine for digital signal processing hardware."

University of California, Berkeley Aug, 1995 – Aug, 1998
B.S. in Electrical Engineering and Computer Sciences
Minor in Music. Graduated with honor.

Research Experience

Graduate Student Researcher Aug 2002 – present
University of California, Berkeley, Prof. Robert Brodersen
Research usability issues of FPGA-based reconfigurable computers (RC's), involving multiple interrelated projects:

- *Operating System*: Developed a general purpose, multi-user operating system (BORPH) for FPGA-based reconfigurable computers. It allows FPGA designs be run as normal UNIX processes under the control of the OS, which provides services such as file I/O and inter-process communications. BORPH provides an intuitive environment for novel users, while preserving the computational power and flexibility of RC's.
- *Design Flow*: Research implications of hardware kernel-user interface on hardware design flow. Participated in the development of a high-level Simulink-based design flow by incorporating BORPH support.
- *Hardware Debugging*: Investigated the possibilities of debugging hardware designs during runtime and their implications on OS design.

Embedded & Reconfigurable Systems Intern Jun 2005 – Oct 2005
Xilinx Research Labs, San Jose, CA, USA
Designed and implemented a Linux virtual file system for performing partial

dynamic reconfigurations of FPGA's. The file system abstraction hide sophisticated runtime manipulation of FPGA configuration needed for FPGA dynamic reconfiguration from users. It handled the capturing and/or modifying of the FPGA's running state. In addition, it handled the discrepancies in access mechanisms for different FPGA constructs, such as lookup tables (LUT's) and on-chip memories (BRAM's), due to physical limitations. The virtual file system presents several views of the FPGA to users:

- *Physical View*: LUT's, flip-flops, and BRAM's of a FPGA are represented as files organized hierarchically in directories corresponding to their Cartesian locations on the chip. Their states and configuration can then be read/modify by standard file system read/write via these virtual files.
- *Logical View*: Virtual files are created according to user specified configuration files corresponding to the running design. The configuration file aggregated physical resources of an FPGA into logical user constructs. As a result, for example, all registers of a user defined counter can then be accessed logically through a single file system read/write.

Graduate Student Researcher Aug 1998 – Aug 2000
University of California, Berkeley, Prof. Robert Brodersen
Research relationship between ASIC design flow and FPGA emulation engine:

- Investigated the initial architecture of a FPGA-based emulation engine, BEE, for use with (1) ASIC emulation and (2) rapid emulation of wireless communication algorithms.
- Took part in implementing a Simulink-based design flow that allows the same high level description of a hardware design be used to generate custom integrated circuits and be emulated with FPGA without major user interventions.

Teaching Experience

Head Teaching Assistant Spring 2006
CS61c: Machine Structures , Prof. John Wawrzynek
An undergraduate class with over 100 students. Responsible for both teaching and administrative tasks.

Teaching Tasks:

- Assisted professor in overall class syllabus planning.
- Gave a lecture on "Reconfigurable Computing".
- Conducted weekly discussion and lab sections.
- Created weekly homework and lab assignments.
- Took part in exam creation.

Administrative Tasks:

- Investigated student conduct issues.
- Handled students lab/discussion section scheduling problem.
- Maintained automatic homework grading system.
- Setup and maintained course website.

Laboratory Teaching Assistant Fall 1999
EE141: Introduction to Digital Integrated Circuits, Prof. Jan Rabaey
Tasks:

- Prepared lab equipment each week.
- Conducted weekly lab section.
- Answered students' questions on course material.

Working Experience

The University of Hong Kong Aug 2007 – persent
Research Assistant Professor Department of Electrical and Electronic Engineering
Research topics related to FPGA-based reconfigurable computing, including integration methodologies between reconfigurable computers and conventional computers, reconfigurable computer architecture, application of reconfigurable computing technologies to high performance computing and high-end embedded systems, and reconfigurable computing education.

Googol Technology (HK) Ltd. Dec 2000 – Aug 2002
Hardware Engineer Hong Kong University of Science and Technology, Hong Kong
Designed and implemented an extensible 8-axis motion controller used for high-precision CNC machines using FPGA technology. Two Xilinx Spartan2 FPGA's were used in each controller. One FPGA was responsible for high precision hardware assisted servo control, PWM generator, ADC, and DAC control. The other FPGA was responsible for central coordination among host PC, an onboard Analog Devices SHARC digital signal processor, and the controlling FPGA.

Awards and Honors

- **California Fellowship in Microelectronics (MICRO)**
  University of California, Berkeley, 1998.
  Awarded to highly qualified first year University of California graduate students for studies in microelectronics and in computer science.
- **Edward Frank Kraft Scholarship Prize**
  University of California, Berkeley, 1995-1996.
  Awarded to freshmen attaining a 4.00 GPA in their first semester.
- Member of **Eta Kappa Nu**, since 1996.

Publications

Journal Papers

[1] H. K.-H. So, and R. Brodersen, "A Unified Hardware/Software Runtime Environment for FPGA-Based Reconfigurable Computers using BORPH." *ACM Transactions in Embedded Computing Systems*, Vol. 7, Issue 2, Feb., 2008, New York, NY, USA.

Conference Papers

[1] D. Markovic, C. Chang, B. Richards, H. So, B. Nikolic and R. Brodersen, "ASIC Design and Verification in an FPGA Environment," to appear in *Proc. of IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2007.

[2] S. Mellers, H. So, B. Richards and R. Brodersen, "A Software Defined Radio Reconfigurable Testbed for Cognitive Radio using BEE2," to appear in *Proc. of the 41st Asilomar Conference on Signals, Systems and Computers*, Nov. 2007.

[3] H. K.-H. So, A. Tkachenko and R. Brodersen, "A unified hardware/software runtime environment for FPGA-based reconfigurable computers using BORPH." in *CODES+ISSS '06: Proceedings of the 4th international conference on hardware/software codesign and system synthesis.* New York, NY, USA: ACM Press, 2006, pp. 259–264.

[4] H. K.-H. So and R. W. Brodersen, "Improving usability of FPGA-based reconfigurable computers through operating system support." in *Proceedings of 2006 International Conference on Field Programmable Logic and Applications (FPL)*, 2006, pp. 349–354.

[5] K. Camera, H. K.-H. So, R. Brodersen, "An integrated debugging environment for reprogrammable hardware systems." in *AADEBUG'05: Proceedings of the sixth international symposium on Automated analysis-driven debugging.* New York, NY, USA: ACM Press, 2006, pp. 111–116.