Si Oxidation

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Typical CMOS Cross-Section
Planar Technology with Multiple Levels
Films on Si

Typical SiO₂ Thickness

- Grown oxide
  - Field oxide: 1µm
  - Diffusion/implant mask: 0.1µm
  - Stress relief/pad oxide: 10nm
  - Gate oxide
  - Native/chemical oxide: 1nm

- Deposited
  - Inter-metal insulation
  - Diffusion/implant mask
Trends for Gate Oxide

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Minimum Feature Size (nm)</td>
<td>250</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>70</td>
<td>50</td>
</tr>
<tr>
<td>DRAM Bits/Chip</td>
<td>256M</td>
<td>1G</td>
<td>4G</td>
<td>16G</td>
<td>64G</td>
<td>256G</td>
</tr>
<tr>
<td>Minimum Supply Voltage (volts)</td>
<td>1.8-2.5</td>
<td>1.5-1.8</td>
<td>1.2-1.5</td>
<td>0.9-1.2</td>
<td>0.6-0.9</td>
<td>0.5-0.6</td>
</tr>
<tr>
<td>Gate Oxide-Two Equivalent (nm)</td>
<td>4-5</td>
<td>3-4</td>
<td>2-3</td>
<td>1.5-2</td>
<td>&lt;1.5</td>
<td>&lt;1.0</td>
</tr>
<tr>
<td>Thickness Control (% 3 ø)</td>
<td>±4</td>
<td>±4</td>
<td>±4-6</td>
<td>±4-8</td>
<td>±4-8</td>
<td>±4-8</td>
</tr>
<tr>
<td>Equivalent Maximum E-field (MV cm⁻¹)</td>
<td>4-5</td>
<td>5</td>
<td>5</td>
<td>&gt;5</td>
<td>&gt;5</td>
<td>&gt;5</td>
</tr>
<tr>
<td>Gate Oxide Leakage (DRAM) (pA µm⁻²)</td>
<td>&lt;0.01</td>
<td>&lt;0.01</td>
<td>&lt;0.01</td>
<td>&lt;0.01</td>
<td>&lt;0.01</td>
<td>&lt;0.01</td>
</tr>
<tr>
<td>Tungsten Oxide (nm)</td>
<td>8.5</td>
<td>8</td>
<td>7.5</td>
<td>7</td>
<td>6.5</td>
<td>6</td>
</tr>
<tr>
<td>Maximum Wiring Levels</td>
<td>6</td>
<td>6-7</td>
<td>7</td>
<td>7.8</td>
<td>8.9</td>
<td>9</td>
</tr>
<tr>
<td>Dielectric Constant, K for</td>
<td>3.0-4.1</td>
<td>2.5-3.0</td>
<td>1.5-2.0</td>
<td>1.5-2.0</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Intermetal Insulator</td>
<td></td>
<td></td>
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</tbody>
</table>

Si Oxidation

- Consumption of Si to form SiO₂
  - Some of the Si near the surface is used to grow Oxide
  - Si-SiO₂ Interface moves down as SiO₂ is grown

- Thermal Oxide: Amorphous; 2.27 g/cm³;
  \( E_g = 9 \text{ eV} \) (Quartz is Crystalline)
Dry and Wet Oxide

- Oxidation Temperature 900 to 1100 °C
- Dry Oxide: Slower Growth Rate, Better Quality
  \[
  \text{Si} + \text{O}_2 \rightarrow \text{SiO}_2
  \]
- Wet Oxide: Faster Growth Rate, Lower Quality
  \[
  \text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2
  \]
Oxidizing Species: $O_2$, $O$, $O^+$, $O^-$, $O_2^+$, ...

1. Transportation from Ambient to Wafer Surface
2. Diffusion from $SiO_2$ Surface to Si-$SiO_2$ Interface
3. Reaction at Si-$SiO_2$

Oxidation Rate - Flux Balance and Interaction at Interface

$x_o^2 + Ax_o = B(t + \tau)$

$x_o = \frac{A}{2} [(1 + \frac{t + \tau}{A^2 / 4B})^{1/2} - 1]$

where $x_o$ = oxide thickness; $t$ = oxidation time

$A = 2D\left(\frac{1}{k_s} + \frac{1}{h}\right)$

with $D$ = Diffusion Constant; $k_s$ = Reaction Rate Constant; $h$ = gas phase mass transfer

$B = \frac{2DC^*}{N_1}$

with $C^*$ = Concentration of Oxidizing Species in $SiO_2$; $N_1$ = Number of Oxidant Molecules. Since $SiO_2$ has $2.2 \times 10^{22}$ molecules/cm$^3$, for $O_2$ oxidation, $N_1 = 2.2 \times 10^{22}$ molecules/cm$^3$ and for $H_2O$ oxidation, $N_1 = 4.4 \times 10^{22}$ molecules/cm$^3$

$\tau = \frac{x_i^2 + Ax_i}{B}$ with $x_i$ = Initial Oxide Thickness
Oxidation Rate Constants

- For Short Oxidation Time – Linear Region
  - \( \frac{B}{A} = \text{Linear Rate Constant, depends on Reaction Rate at Interface} \)
    - \( (t + \tau) \ll \frac{A^2}{4B} \)
    - \( x_o \approx \frac{B}{A} (t + \tau) \)
    - \( \frac{B}{A} = \frac{kC^*}{N_i} \)

- For Long Oxidation Time – Parabolic Region
  - \( B = \text{Parabolic Rate Constant, Oxidation limited by Diffusion} \)
    - \( t \gg \tau \)
    - \( x_o^2 \approx Bt \)

Oxidation Rate Varies with Time

- Both Rate Constants (\( \frac{B}{A} \), \( B \)) increase with Temperature - Faster for Wet Oxidation compared to Dry Oxidation

<table>
<thead>
<tr>
<th>Temperature</th>
<th>( \frac{B}{A} ) (( \mu \text{m/h} ))</th>
<th>( B ) (( \mu \text{m}^2/\text{hr} ))</th>
<th>( \tau ) (hr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000°C Dry</td>
<td>0.071</td>
<td>0.0117</td>
<td>0.37</td>
</tr>
<tr>
<td>1000°C Wet</td>
<td>1.27</td>
<td>0.287</td>
<td>0</td>
</tr>
<tr>
<td>1200°C Wet</td>
<td>14.4</td>
<td>0.72</td>
<td>0</td>
</tr>
</tbody>
</table>
**Oxidation Rate Constants**

- B/A Linear Rate Constant - Reaction Rate at Interface
- B Parabolic Rate Constant - Diffusion

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**Si Wafers in Oxidation Furnace**

Horizontal furnace
**Color Chart for Si$_3$N$_4$ Thickness**

<table>
<thead>
<tr>
<th>Film Thickness (nm)</th>
<th>Color</th>
<th>Film Thickness (nm)</th>
<th>Color</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>Light brown</td>
<td>95</td>
<td>Light blue</td>
</tr>
<tr>
<td>17</td>
<td>Medium brown</td>
<td>105</td>
<td>Very light blue</td>
</tr>
<tr>
<td>25</td>
<td>Brown</td>
<td>115</td>
<td>Light blue-brown</td>
</tr>
<tr>
<td>34</td>
<td>Brown-pink</td>
<td>125</td>
<td>Light brown-yellow</td>
</tr>
<tr>
<td>35</td>
<td>Pink-purple</td>
<td>135</td>
<td>Very light yellow</td>
</tr>
<tr>
<td>43</td>
<td>Purple</td>
<td>145</td>
<td>Light yellow</td>
</tr>
<tr>
<td>53</td>
<td>Very dark blue</td>
<td>155</td>
<td>Yellow</td>
</tr>
<tr>
<td>60</td>
<td>Dark blue</td>
<td>165</td>
<td>Bright yellow</td>
</tr>
<tr>
<td>70</td>
<td>Medium blue</td>
<td>175</td>
<td>Intense yellow</td>
</tr>
</tbody>
</table>

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**Factors that Affect Oxidation - I**

- **Crystal Orientation**
  - Oxidation Rate for (111) > (110) > (100)
  - B – Little Dependence on Orientation since diffusion through oxide is not affected by Si orientation
  - B/A – Oxidation Rate Ratio (111)/(100) ~ 1.68 Reaction Rate at Si-SiO$_2$ interface depends on number of Bonds available for Oxidation; (111) – 1.18x10$^{15}$ cm$^{-2}$; (100) – 6.77x10$^{14}$ cm$^{-2}$
  - Less Crystal Orientation Dependence at Higher Temperature or Longer Time since the oxidation is limited by Diffusion in Parabolic region

- **Dopant Effects**
  - Dopants (B, As, P, ...) Enhance Oxidation Rate
  - For B: B Piles up in SiO$_2$, weakens SiO$_2$ Structure and enhances Diffusion of Oxidant
  - For P: P Piles up in Si. Linear Rate Constant (B/A) becomes faster, not much effect on B
  - Heavy Doping causes E$_F$ to shift, which increases Vacancies in Si. This provides more Reaction Sites for Oxidation
Factors that Affect Oxidation - II

- **H₂O Effect (Dry vs. Wet Oxidation)**
  - H₂O Increases Oxidation Rate with Lower Quality Oxide and more Defects
  - Both B/A and B increase for Wet Oxidation
  - Faster Reaction Rate at SiO₂-Si Interface
  - Larger Amount of Oxidant Allowed in SiO₂: C* for H₂O – 3x10¹⁹ cm⁻³; C* for O₂ – 5.2x10¹⁶ cm⁻³

- **Halogen Effect (Cl₂ or F-based)**
  - 1-5 % HCl Addition
  - Increases Oxidation Rate since HCl reacts with O₂ to from H₂O
  - Converts Impurities in Si (e.g. Na, Fe, …) to form Volatile Products: Reduce Metallic Impurity Concentration and Defects in Oxide; Improve Breakdown Voltage and Lifetime

Factors that Affect Oxidation - III

- **Pressure Effect**
  - **High Pressure Oxidation**
    - 10-25 atm, 600-1200 °C
    - Increases Vertical Growth Rate faster than Lateral Growth Rate
    - Oxide can be grown at Lower Temperature (Temperature reduced by 30 °C with increase of 1 atm)
    - Reduce Bird’s Beak Encroachment
  - **Low Pressure Oxidation**
    - 10⁻² to 1 atm, 800-1000 °C
    - Reduce Rate for Thin Oxide
    - Higher Oxide Quality to grow at Lower Pressure than Lower Temperature
    - Oxidation rate ~ P₀.⁸
Faster Oxidation Rate at Higher Pressure

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Oxidation to Isolate Devices

- ~30% Volume Expansion when Oxide is Formed
- Defects Around Bird’s Beak
- Recess Oxide to Reduce Topography
Dopant Distribution at Interface

- Dopant Re-Distribute until Chemical Potential is the same on each side of Interface
- Can Affect $V_T$ due to change in Channel Doping
- Segregation Coefficient $m = \frac{\text{Dopant in Si}}{\text{Dopant in SiO}_2}$
- Examples: (Dry Oxidation, 950 °C; Left: B in Si; Right: P in Si)

\[
\text{Dopant Distribution at Interface}
\]

\[m = \frac{C_{\text{Si}}}{C_{\text{SiO}_2}}\]

Dopants In Oxide and Near Interface

- m<1, slow oxide diffusion: e.g. B
- m<1, fast oxide diffusion: e.g. B with H
- m>1, slow oxide diffusion: e.g. P
- m>1, fast oxide diffusion: e.g. Ga
**Thin Oxide (<30 nm)**

- Grown at Lower Temperature, Lower Pressure, Rapid Thermal Oxidation (RTO), or Plasma-Assisted Oxidation
- Deal-Grove Model: OK for Wet Oxidation ($\tau = 0$); Faster Initial Growth Rate, Adjusted by having $\tau > 0$
- For Thin Oxide, Oxidation Rate decreases exponentially with thickness:

  $\frac{dx_{ox}}{dt} = \frac{B}{2x_{ox}} + A + C_1 e^{-x_{ox}/L_1} + C_2 e^{-x_{ox}/L_2}$

  From D-G Excess Rate
  Decay Length: $L_1 \sim 5$ nm; $L_2 \sim 7$ nm
- Si Surface with Additional Sites for Oxidation. These sites decrease exponentially into Si with decay length of ~3 nm. These sites enhance oxidation
- Blocking Layer SiO causes accumulation of Oxygen that can transform rapidly to SiO$_2$

**Ultra Thin Gate Oxide (<5 nm)**

- Problems
  - Large Leakage Current (e.g. at 1V, 1x10$^{-12}$ A/cm$^2$ for 3.5 nm, 10 A/cm$^2$ for 1.5 nm)
  - Defects in Oxide and Interface
  - Control of Oxide Thickness
  - Dopant Penetration from Doped Poly-Si Gate
- Approaches
  - Nitrided Films (Oxide-Nitride, Oxide-Nitride-Oxide, Oxynitride, …)
  - High k Dielectrics ($\varepsilon_{SiO_2} = 3.9$; $\varepsilon_{Si_3N_4} = 7.5$; $\varepsilon_{Ta_2O_5} = 25$; $\varepsilon_{TiO_2} = 50$; $\varepsilon_{SrTiO_3} = 150$, …)

  Equivalent Oxide Thickness (compared to SiO$_2$ with $\varepsilon = 3.9$)
  For $x_{eq} = 3$ nm and with $\varepsilon_{SiO_2} = 3.9$, $\varepsilon_{TiO_2} = 50$:

  $x_{TiO_2} = \frac{x_{eq} \varepsilon_{TiO_2}}{\varepsilon_{SiO_2}} = 38.5$ nm

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Alternative Oxides

- Thermal Oxidation with NO, N₂O, O₂ re-oxidation of oxynitrides
  HF/H₂O Vapor
  - NO – Oxynitride, Self-Limiting Growth since nitrogen rich oxide is a diffusion barrier
  - N₂O – Reduce to NO and O which grow oxide with N Close to Si–SiO₂ Interface: NO – Nitrogen in Oxide; O – Remove N in Oxide near Surface
  - O₂ Anneal of Oxynitride – Forms SiO₂ at Interface with Oxynitride near Surface

- Plasma–Assisted Oxidation
  - Remote Plasma to Activate O₂, N₂O, N₂, NH₃, ...
  - Lower Thermal Budget
  - Typical Condition for Oxidation/Nitridation: 300 °C, 300 mTorr, <1 min; Annealing at 900 °C, 30 s
  - N Tends to Locate Close to Si–SiO₂ Interface with ~1 monolayer N (7x10¹⁴ cm⁻²) after 90 s plasma exposure when remote plasma at higher pressure (~300 mTorr) and N₂O is used
  - N Tends to be at Top Surface when N₂ is used at lower pressure (~100 mTorr)
  - Effective in Lowering Leakage Current and Blocking B Diffusion from Poly-Si Gate

Oxide-Nitride Stacks

- Advantages of Nitride
  - Interface Nitridation Lower Leakage Current
  - Bulk Nitride Allows Increased Physical Thickness
  - Top-Surface Nitride Block Dopant Diffusion from Poly-Si Gate

- Disadvantages of Nitride
  - Film Stability
  - Positive Charges and Defects in Nitride tend to vary when Bias is Applied
  - Worse Stability and Reliability of Nitride as Gate Dielectric
**High k Dielectrics**

- Allows Thicker Film to Lower Leakage Current - Fowler-Nordheim Tunneling Current Increases Exponentially with Reduced Thickness or Reduced Barrier Height
- Needs Thicker Film with Larger Barrier Height
- Needs Thermally Stable Film (most high k films form SiO<sub>2</sub> on Si)
- Needs to develop New Etching Techniques
- Silicates and Oxide of Hafnium and Zirconium - HfSiON, HfO<sub>2</sub>, HfSiO, ....

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**Properties of Insulators**

<table>
<thead>
<tr>
<th>Structure</th>
<th>SiO&lt;sub&gt;2&lt;/sub&gt;</th>
<th>Si&lt;sub&gt;3&lt;/sub&gt;N&lt;sub&gt;4&lt;/sub&gt;</th>
<th>SiO&lt;sub&gt;x&lt;/sub&gt;N&lt;sub&gt;y&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amorphous</td>
<td>Amorphous</td>
<td>Amorphous</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Resistivity (Ωcm)</td>
<td>10&lt;sup&gt;4&lt;/sup&gt; – 10&lt;sup&gt;6&lt;/sup&gt;</td>
<td>≈ 10&lt;sup&gt;4&lt;/sup&gt;</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Density (gm cm&lt;sup&gt;-3&lt;/sup&gt;)</td>
<td>2.27</td>
<td>3.1</td>
<td></td>
</tr>
<tr>
<td>Dielectric constant, K</td>
<td>3.8 – 3.9</td>
<td>7.5</td>
<td>5 – 6</td>
</tr>
<tr>
<td>Dielectric strength (V cm&lt;sup&gt;-1&lt;/sup&gt;)</td>
<td>5 – 10 × 10&lt;sup&gt;6&lt;/sup&gt;</td>
<td>≈ 10&lt;sup&gt;3&lt;/sup&gt;</td>
<td>≈ 5 × 10&lt;sup&gt;6&lt;/sup&gt;</td>
</tr>
<tr>
<td>Energy gap (eV)</td>
<td>≈ 9</td>
<td>≈ 5</td>
<td></td>
</tr>
<tr>
<td>Expansion coeff. (°C&lt;sup&gt;-1&lt;/sup&gt;)</td>
<td>5 × 10&lt;sup&gt;-1&lt;/sup&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Refractive index</td>
<td>1.46</td>
<td>2.05</td>
<td>1.6 – 1.9</td>
</tr>
<tr>
<td>Thin film stress (dyne cm&lt;sup&gt;-2&lt;/sup&gt;)</td>
<td>2 – 4 × 10&lt;sup&gt;9&lt;/sup&gt;</td>
<td>9 – 10 × 10&lt;sup&gt;9&lt;/sup&gt;</td>
<td>1 – 6 × 10&lt;sup&gt;9&lt;/sup&gt;</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm&lt;sup&gt;2&lt;/sup&gt;°C)</td>
<td>0.014</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Infrared absorption peak (µ)</td>
<td>9 - 3</td>
<td>11.5 – 12</td>
<td>9 – 12</td>
</tr>
<tr>
<td>Etch rate in buffered HF (nm min&lt;sup&gt;-1&lt;/sup&gt;)</td>
<td>100</td>
<td>0.5 – 1</td>
<td>2 – 40</td>
</tr>
<tr>
<td>Melting point (°C)</td>
<td>≈ 1700</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electron mobility (cm&lt;sup&gt;2&lt;/sup&gt; volt&lt;sup&gt;-1&lt;/sup&gt; sec&lt;sup&gt;-1&lt;/sup&gt;)</td>
<td>20 – 40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hole mobility (cm&lt;sup&gt;2&lt;/sup&gt; volt&lt;sup&gt;-1&lt;/sup&gt; sec&lt;sup&gt;-1&lt;/sup&gt;)</td>
<td>≈ 2 × 10&lt;sup&gt;-5&lt;/sup&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Surface conductivity (Ω/sq)</td>
<td>10&lt;sup&gt;9&lt;/sup&gt; – 10&lt;sup&gt;15&lt;/sup&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>